Publishable Summary

PHASTFlex: Photonic Hybrid ASsembly Through Flexible waveguides

PHASTFlex proposes the development of a fully automated, high precision, cost-effective assembly technology for next generations of hybrid photonic packages.

Background

PHASTFlex is engaged in the development of a fully automated, high precision, cost-effective assembly technology for next generation hybrid photonic packages. Multiple Photonic ICs (PICs) will be assembled in hybrid packages combining the best of different material platforms for a wide range of applications and performance. In PHASTFlex, InP PICs with active functions will be combined with passive TriPleX PICs.

PIC fabrication can now be done using generic foundry-based processes[1], bringing the cost of an application specific PIC (ASPIC), into the range ~10-100€, which is within the scope of many applications developers. However, current assembly and packaging technology still leads to custom-engineered solutions thereafter; packaging is an order of magnitude more expensive, and this is a major bottleneck to further market penetration.

The most demanding assembly task for multi-port PICs is the high-precision (±0.1µm) alignment and fixing required for optical I/O in InP PICs, even with waveguide spot size conversion. PHASTFlex proposes an innovative concept, in which the waveguides in a matching TriPleX PIC are released during fabrication to make them movable. Actuators and fixing functions, integrated in the same PIC, place and fix the flexible waveguides in the optimal position (peak out-coupled power).

The project aims for proof of concept for a complete assembly process and the required tooling to implement this approach, including pre-assembly using solder reflow and automated handling, and on-chip micro-fabricated fine-alignment and fixing functions, for real end user applications.

The consortium believes that such a fully automated cost-effective and high-performance solution will also encourage photonic packaging to be carried out in EU economies rather than shipped to the low wage economies of the Far East.

Technical achievements

The overall concept for the PHASTFlex subassembly is schematically depicted in Figure 1 (left) visualizing the assembly layout in a 3D view. An InP and a TriPleX photonic chip connected to a fiber array unit are passively assembled on an LTCC carrier. Greater detail on the fine tuning of the alignment concept can be seen on the right part of the figure. Position tuning in two directions is achieved by actuation of flexible waveguide fingers on the TriPleX platform. Flexible waveguide beams are released by etching the supporting silicon. The beams are connected by a cross-bar at their ends. To move the waveguide array, bimorph actuators are

[1] *See for example the JePPIX website www.jeppix.eu and information therein.*

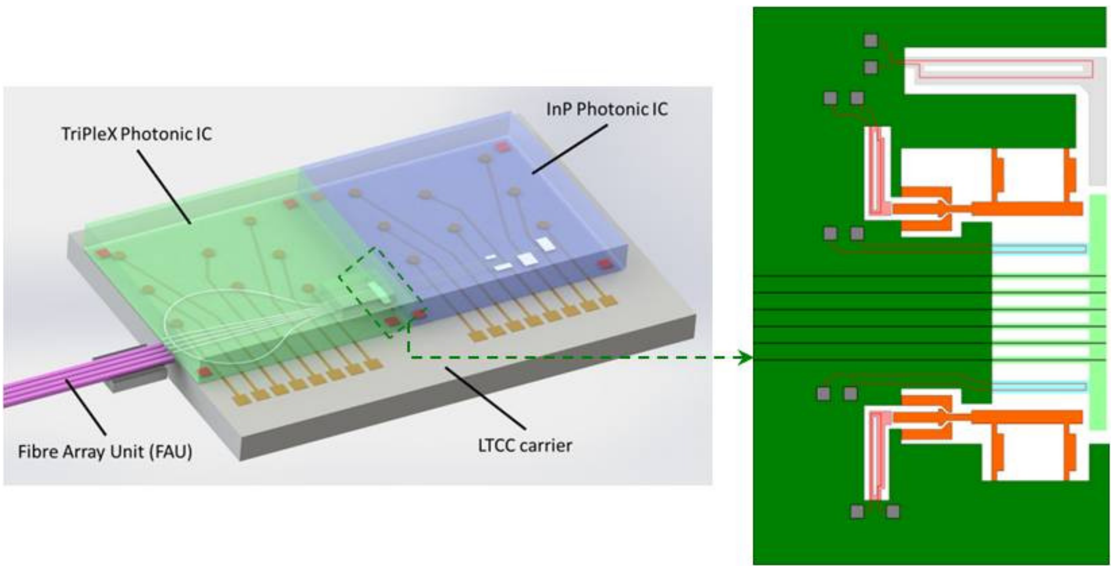

Figure 1: 3D view of the overall assembly concept proposal (left) and proposed MEMS-based fine alignment functions on TriPleX PIC in more detail (right).

used for out-of-plane translation and rotation around the propagation direction. A U-beam actuator generates in-plane translation. Once at the correct position the T-bar connecting the fingers is clamped utilizing a MEMS-based fixing concept.

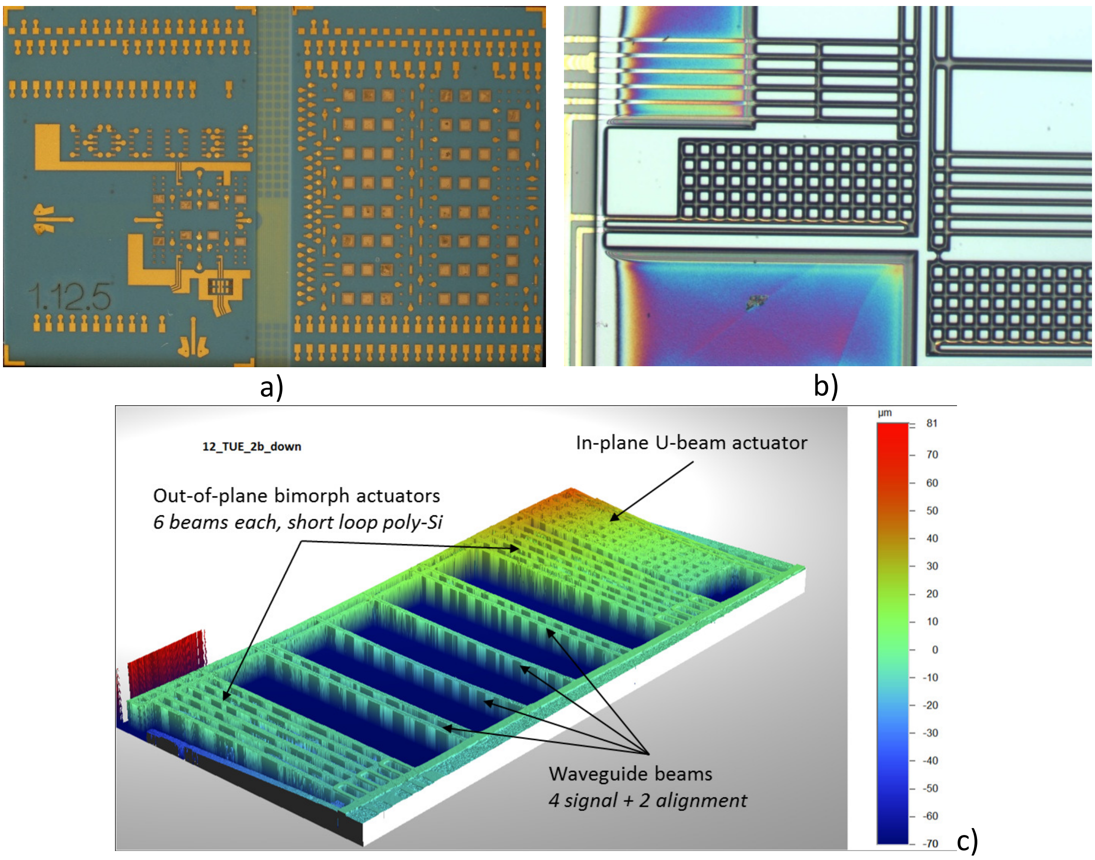

Figure 2: Photograph of fabricated LTCC carrier (a), fabrication snapshot of MEMS on TriPleX chip (b) and white light interferometry image showing 3D profile of MEMS functions (c).

In the first half of the project the design concepts have been refined and the assembly as well as the TriPleX MEMS requirements quantified in order to enable the design and realization of the first matching chip set suitable for assembly trials on a common carrier. In parallel the assembly concept has been developed to match the applications requirements. The design of the assembly machine was completed and all parts for the machine and assembly kit have been procured. The assembly machine is finalized, calibrated, tested and delivered. The fabrication of all chip and carrier piece parts is completed; preliminary results of assembly tests are available.

An LTCC carrier which accepts all combinations of the matching InP and TriPleX chips, and provides for the necessary DC and RF interconnects between the probe cards and the active circuit elements has been designed and realized (Figure 2a). The implementation of the MEMS layouts on the TriPleX chips can be seen from the fabrication snapshot in Figure 2b. A 3D image of the realized actuator functions on a TriPleX chip taken by white light interferometry is depicted in Figure 2c.

The assembly machine is designed to allow oven bonding of the InP and the TriPleX chips to the LTCC carrier as well as to allow active alignment of the MEMS structures of the TriPleX chip through probe cards and contact pads designed into the LTCC. 3D drawings of the assembly unit are shown in Figure 3. Examples of first TriPleX chip assemblies to LTCC carriers utilizing the assembly machine can be seen from the photograph in Figure 4.

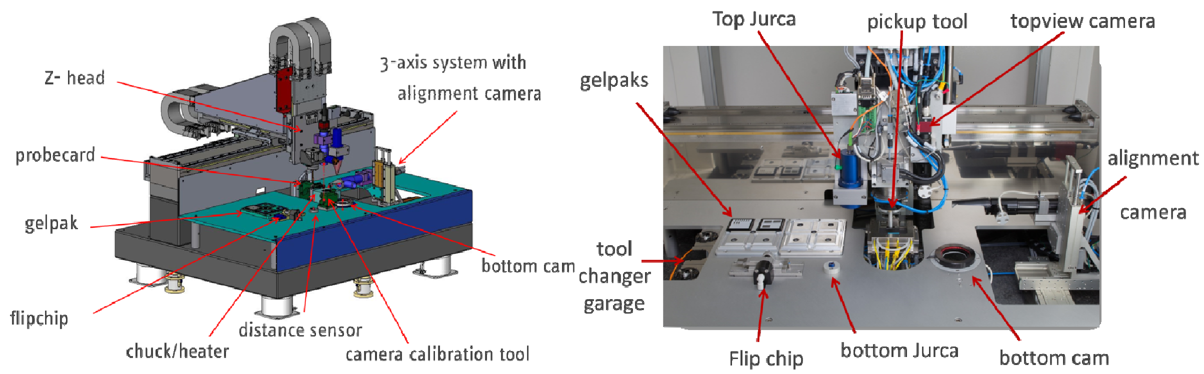

Figure 3(Left) Assembly machine. 3D-model of the alignment module with flip-chip station, oven with probing mechanism, alignment camera and force controlled bond-head including an optical distance sensor (Right) Photograph of the interior of the assembly machine

PHASTFlex has already made one large step forward in the proposed technology with the provision of the necessary co-designed piece-parts, and exploration of the capabilities of the assembly machine can now begin in earnest, pushing on towards our target initial placement accuracy for the two PICs of 1.5 +/-0.5 µm. In parallel, second cycle MEMS process runs will be pushed through in the near term to stabilise process flows, improve yield and provide more samples. The applications focus of the period two programme will see a second iteration of designs in TriPleX and InP targeting PICs for specific applications in communications which will be used to further prove out the concept

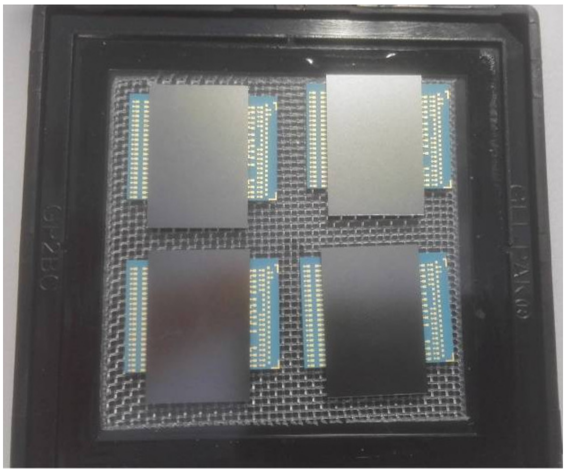

Figure 4 Photograph of first TriPleX test chips assembled to LTCC carriers

General project facts and figures

The website address for the project is http://phastflex.eu

Ref: FP7-ICT 619267 PHASTFlex

European Commission

Partners in the PHASTFlex consortium are:

- TU Eindhoven (Coordinator)
- TU Delft
- Oclaro Technology Ltd.
- LioniX BV
- Willow Photonics Ltd.
- AifoTEC AG
- FiconTEC GmbH
- IMST GmbH
- TELNET Redes Intelligentes SA

For further project information, please contact:

David Robbins
Willow Photonics
Tel: +44 (0)1327 857795
E-mail: dave.robbins@willowphotonics.co.uk

Xaveer Leijtens
COBRA, TU Eindhoven
Tel: + +31 40 247 5112
E-mail: X.J.M.Leijtens@tue.nl