PHASTFlex

Photonic **H**ybrid **AS**sembly
Through **FLEX**ible waveguides

Newsletter #1 | April 2015

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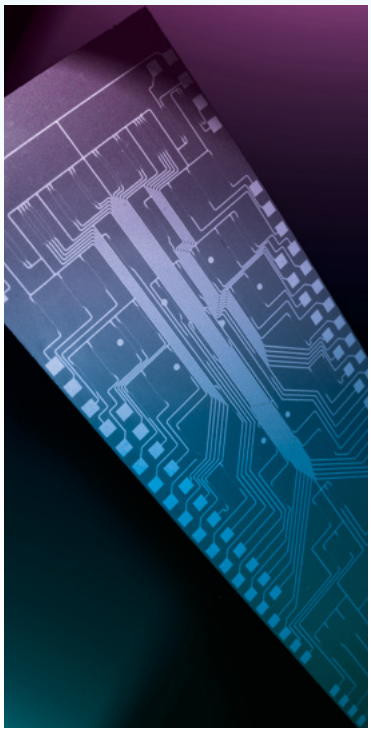
About PHASTFlex

Optical chips, chips that work with light signals instead of electronic signals, are in increasing demand, for example to help process ever-growing internet traffic flows. They are often referred to as Photonic Integrated Circuits (PICs).



What is less well known is that they also have great potential in many other application areas. It is now widely recognized that the ever larger data flows in computers, in data centres and in processors with dozens of arithmetic cores require optical components as well; and low cost PIC based readout units for fibre based structural sensors could revolutionize engineering approaches in wind turbines, aeronautics and in structural engineering.

▶ read more...

General facts and figures

PHASTFlex proposes the development of a fully automated, high precision, cost-effective assembly technology for next generations of hybrid photonic packages.

Project Start Date:
January 1st 2014. The project duration will be of three years, and the cost will be close to 4M€

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Website: www.phastflex.eu

EU funded project

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PHASTFlex

The consortium, which is led by TU Eindhoven in collaboration with LioniX BV in the Netherlands and Willow photonics in the UK, consists of nine partners in total; seven industrial (LioniX bv, Oclaro Technology Ltd, IMST GmbH, TELNET Redes Intelligentes SA, Willow Photonics Ltd, AifoTec GmbH and FiconTec GmbH) of which two provide applications (Oclaro, TELNET), and two are universities (TU Delft, TU Eindhoven). All are recognized to be leading industrial and research entities in the photonics components and systems industry.

1. About PHASTFlex (continued from page 1)

A long standing problem in the deployment of optical circuits based on Indium Phosphide materials has been the small size of the optical waveguides compared to the standard transmission medium – glass optical fibre. High-precision, sub micron alignments are needed, which makes packaging, which achieves the coupling of the light from the PIC to the optical fibre and hence the outside world, expensive. The PHASTFlex project focuses specifically on finding a solution to this technical problem.

PHASTFlex proposes the development of a fully automated, high precision, cost-effective assembly technology for next generation hybrid photonic packages. In hybrid packages, multiple PICs can be assembled, combining the best of different material platforms for a wide range of applications and performance. In PHASTFlex, InP PICs with active functions will be combined with passive TriPleX™ PICs on a ceramic carrier as shown schematically in Figure 1. The most demanding assembly task for multi-port PICs is the high-precision (±0.1µm) alignment and fixing of the optical waveguides. The PHASTFlex consortium proposes an innovative concept, in which the waveguides in the TriPleX PIC are released during fabrication to make them movable. A two stage assembly process is envisaged in which a passive placement and bonding stage is followed by an active fine alignment stage using integrated MEMS functions on the TriPleX chip after which the waveguides can be locked in position. Actuators and fixing functions, integrated in the same PIC, place and fix the flexible waveguides in the optimal position (peak out-coupled power) with the accuracy required.

The PHASTFlex project aims to develop a complete assembly process and the necessary tooling to implement this concept, including pre-assembly using solder reflow and automated handling, and on-chip micro-fabricated fine-alignment and fixing functions. It is worth noting that the availability of fully automated cost-effective and high-performance solutions may also encourage providers of photonic packaging services to locate in EU economies rather than in the Far East in the future.

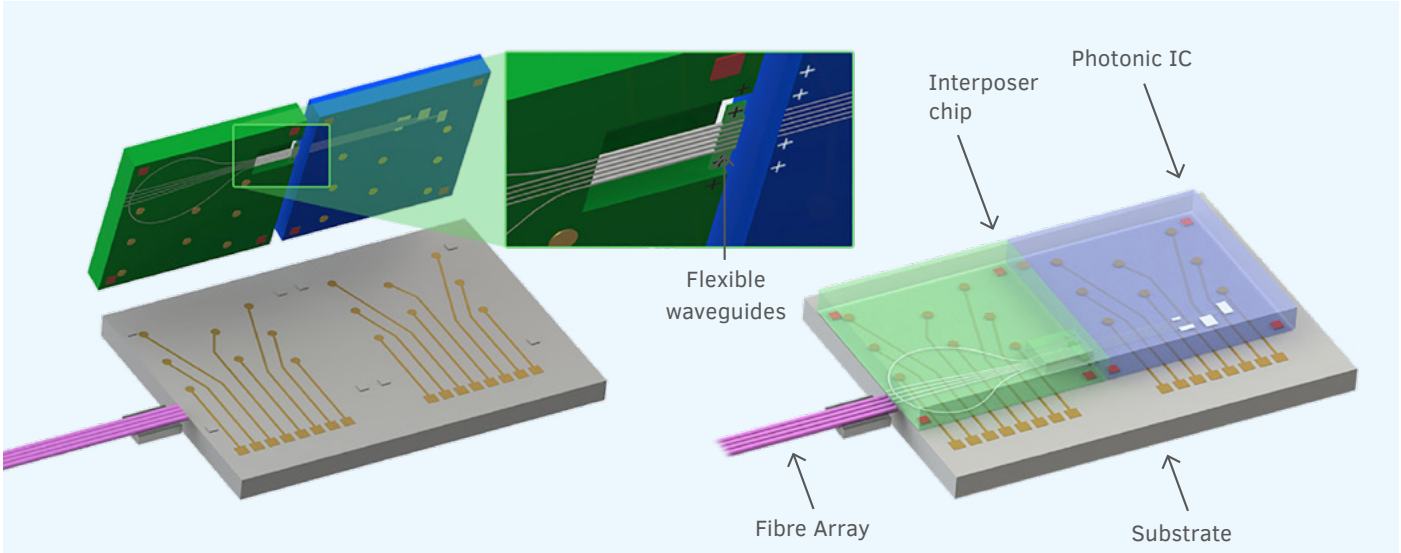


Figure 1 The overall package concept proposal, and detail of PIC interface and on-chip TriPleX fine alignment functions design.

PIC fabrication can now be carried out in a generic foundry-based process, bringing PIC cost within the scope of many applications (~10-100€ per chip). However, current assembly and packaging technology leads to custom-engineered solutions; so packaging remains an order of magnitude more expensive. The Photonics21 Strategic Research Agenda refers to photonics packaging technology as a short term research priority[1].

In PHASTFlex, partners Telnet and Oclaro are working on developing leading edge PIC applications which can take advantage of, and test, this new technology. InP PICs are ideally suited for transmitter applications offering high performance integrated laser sources and high speed detectors. TriPleX PICs offer ultra-low loss waveguides and optical multiplexing and de-multiplexing functions.

1 http://www.photonics21.org/download/sra_april.pdf

2. Flexible Waveguides

The fine-alignment of waveguides is done using MEMS functionality, and here PHASTFlex is partnering with the Dutch STW Flex-o-Guides project to develop actuated flexible waveguide technology which is integrated into the TriPleX chip. MEMS stands for MicroElectroMechanical System, and refers to design and fabrication technology to realise micro-scale “machines”, using (silicon) microfabrication technology. In the PHASTFlex project, three MEMS-based functions are needed:

- Mechanically flexible waveguide structures;
- Actuators which operate on the flexible waveguide structures to bring them in position accurately;
- Fixing functions, to lock the flexible waveguide structures in place once the optimum position is found in an active alignment scheme.

The demands on the MEMS functions and the fine-alignment are high. PHASTFlex aims at deep sub-µm precision in alignment (100-300nm). A variety of waveguide layouts (number of optical ports, port pitch) must be accommodated. The actuators must have a travel range in the order of 5-10µm in order to compensate the error after chip placement and bonding. Also, the space consumption of the actuator and fixing functions must be compatible with the overall chip design and space availability.

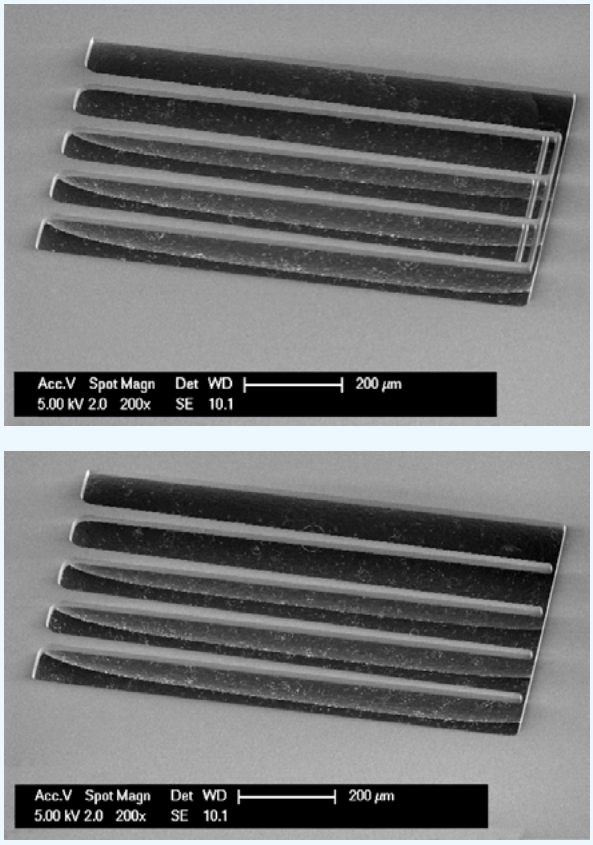


Figure 2 The picture shows released waveguide beams: individual beam (left) and beams coupled with a cross-bar at their ends (right) [courtesy Tjitte-Jelte Peters, TU Delft].

The fabrication of all the functions must be compatible with the TriPleX chip design and fabrication process.

One challenge TU Delft has been working on is the development of a reliable fabrication process for flexible waveguide structures. The TriPleX waveguide consists of silicon oxide claddings of substantial thickness (e.g. 16 µm total stack height) with a silicon nitride waveguide core, realised on a silicon wafer. The length of the flexible guides can be 500µm to even 1000µm, leading to quite slender, high aspect ratio structures. A process is now available to release thick oxide structures as shown in figure 2.

In the first phase of the project focus has been on refining the design concept and quantifying the assembly steps, and on the TriPleX MEMS requirements introduced in the first section. Decisions made here have led to the start of fabrication of the first matching chip set suitable for assembly trials. In parallel the assembly concept has been developed to match the applications requirements and the assembly machine design completed using the mechanical design package Solid Works. Parts needed for the build of this machine are currently being procured, together with various larger pieces of equipment, such as cameras, which are part of the assembly kit.

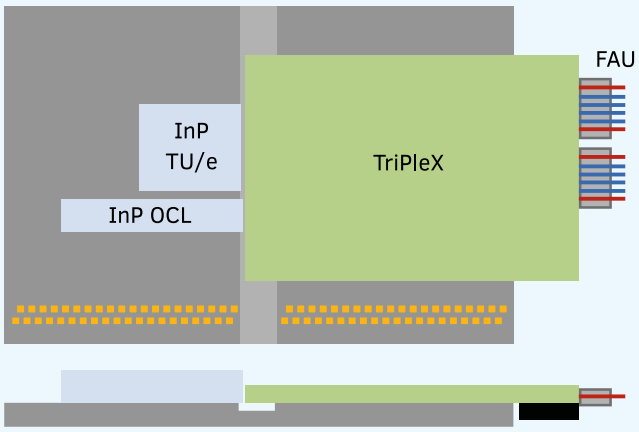
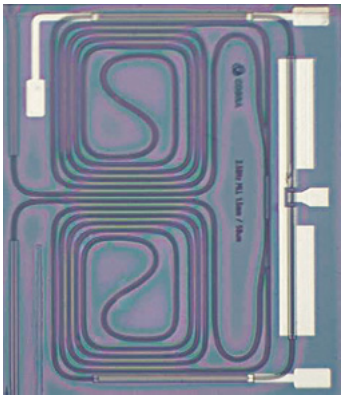


Figure 3 shows in plan and cross-section views the layout of the chips although in practice we will only assemble one InP chip at a time. The fibre array attach using a glass support rail is also shown.

The overall concept for the PHASTFlex subassembly is shown in Figures 1 and 2. In Figure 3 the geometrical arrangements of the chips when assembled are shown more accurately.

InP-based photonic integrated circuits



ASPIC: An Application Specific Photonic Integrated Circuit fabricated in InP; the photonic equivalent of micro-electronic ASIC allowing integration of multiple passive and active photonic components within a single chip, enabling the manipulation of light intensity, wavelength, phase and polarisation in photonics integrated circuits.

Applications: telecommunication, datacomm, sensor systems and fibre sensors, microwave systems, medical, bio-imaging and diagnostics, metrology, and many more...

Advantages: compact, highly integrated, multifunctional, high-speed, energy-efficient, lower cost of fabrication and packaging.

3. Thermo-mechanical design

For the actuation of the flexible waveguide structures, thermal actuators are proposed. These actuators can in principle deliver the required stroke, precision and force. In order to get a better understanding of the feasibility of the design, a parametrised numerical model has been realised in COMSOL to estimate the stiffness and deformation of the waveguide structure, see picture. The six middle beams represent the free hanging waveguides, the beams to the left and right of the waveguide structure are bimorph beams which allow translation of the structure out of plane and rotate the structure around the propagation direction. Two of the key parameters are the free length and the pitch of the waveguide structures. Varying these as well as other parameters gives insight in the stiffness of the structure, the requirements on the actuators, and the alignment precision that can be achieved. The picture to the right shows a temperature map; in this example the bimorph actuators to the left are driven. The information from the modelling will be used to define a suitable design for the overall MEMS functions.

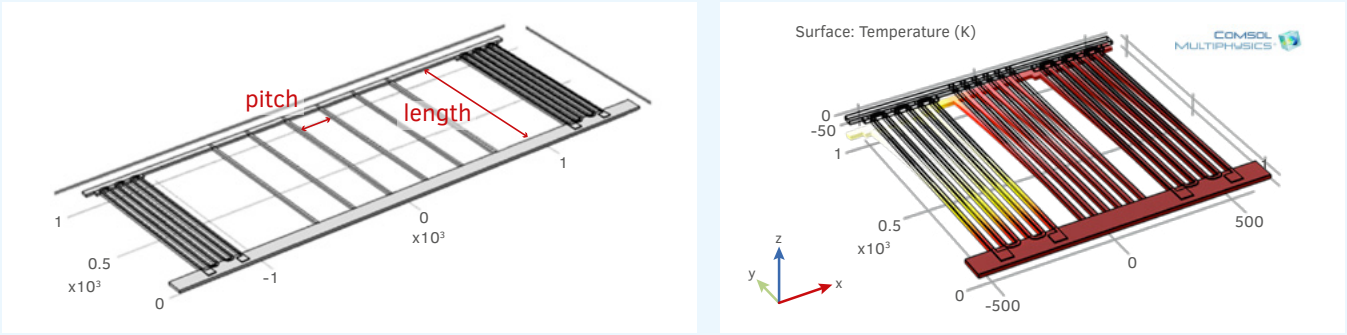


Figure 4 Waveguide and T-bar structures in a parameterised COMSOL model. *Left*: Parameterised geometric model. The waveguides are the beams in the middle of the design, to the left and right actuator structures are included. *Right*: modelled temperature distribution for an array of actuators showing an operating temperature rise of ~300°C from cool (red) to hot (white).

4. Chip bonding on carrier

In the first phase of the project focus has been on refining the design concept and quantifying the assembly steps, and on the TriPleX MEMS requirements introduced in the first section. Decisions made here have led to the start of fabrication of the first matching chip set suitable for full assembly trials. In parallel, the assembly concept has been developed to match the applications requirements and the assembly machine design completed using the mechanical design package Solid Works. In Figure 5 an exploded drawing of the proposed assembly showing the piece parts required is shown in their approximate spatial relationship.

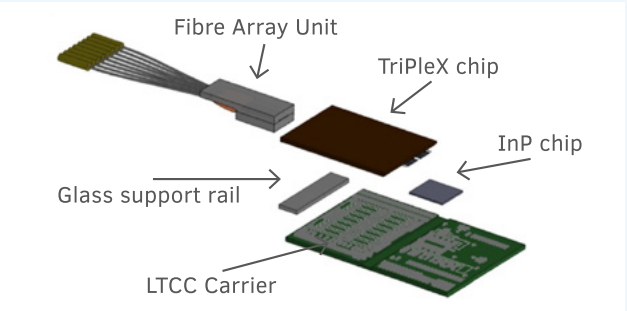


Figure 5 Exploded drawing of assembly showing the piece parts required (from left to right) Fibre array unit, TriPleX chip (backside view), glass rail, InP chip (TU/e test chip, backside view), LTCC carrier (top view).

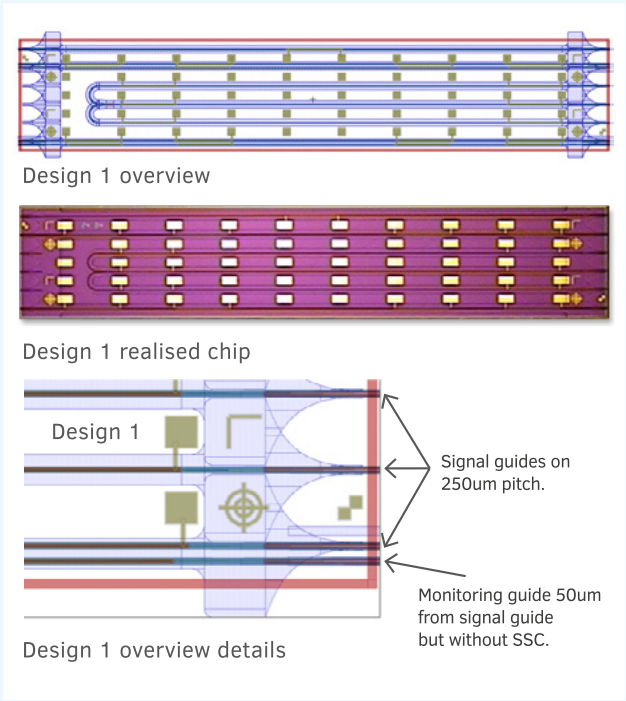


Figure 6 InP test chip designed and fabricated by Oclaro.

A LTCC (Low Temperature Co-fired Ceramic) carrier has been designed by IMST which accepts all combinations of matching InP (Oclaro and TU/e) test chips and TriPleX (LX) chips, and provides for the necessary DC and RF interconnects between the probe cards and the active circuit elements.

In these first trials separate provision is made for the InP PICs of Oclaro and TU/e. These subcomponents have waveguide patterns which are designed to match the TriPleX chips, accommodating the variety of InP chips as well as variants of MEMS designs.

These chips will enable us to test the alignment mechanism of the MEMS actuators using various loopback waveguide arrangements on the TriPleX chip and an external source.

5. Automated assembly machine

The industrial prototype of an assembly machine will consist of a 4-axis manipulator, with nozzles for chip handling and sensor systems for process control. A vision system will be used to support the alignment. The machine will be used for single package assembly and contain functions for solder reflow of the PICs; to target passive alignments to better than ±0.5µm will require state-of-the-art or better machine.

An alignment machine for assembling the three components has been designed; 3D drawings of the proposed machine are shown in Figure 7 right, and parts are currently being procured. The machine is designed to allow oven bonding of the InP and the TriPleX chips to the LTCC carrier, as well as to allow active alignment of the MEMS structures of the TriPleX chip through probe cards and contact pads designed into the LTCC.

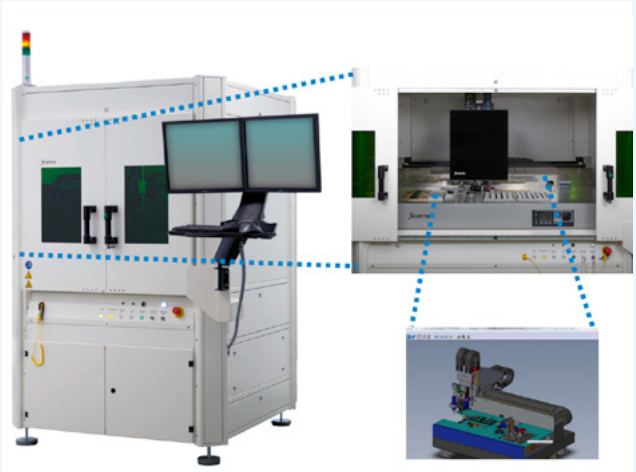
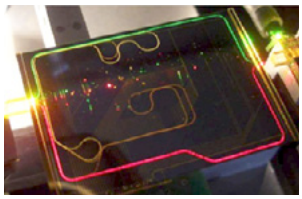


Figure 7 (Left) Typical assembly machine (FiconTEC) and (Right) detail of interior structure.

In the coming year PHASTFlex aims to demonstrate this new assembly technique in a dedicated bonding machine at partner Aifotec.

The TriPleX platform of LioniX is one of the three main photonic platforms next to InP and Silicon On Insulator (SOI).



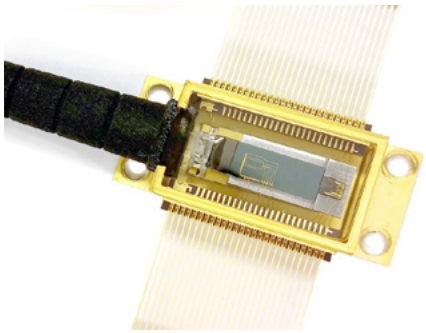
The TriPleX waveguides are based on Low Pressure Chemical Vapour Deposition (LPCVD) of Si_3N_4 and SiO_2. Both materials have stable properties and can be grown in batches making the technology extremely stable and suitable for volume applications. The unique selling point of the technology is the low propagation loss of the waveguides, which makes TriPleX highly complementary to InP PICs. Propagation losses of 0.1 dB/cm for high contrast waveguides, and 0.001 dB/cm for low contrast waveguides, have been measured. The technology is offered via Multi-Project Wafer runs in the same software environment as the InP technology allowing also multi-platform design in hybrid combinations.

www.lionixbv.nl/triplexmpw

JePPIX stands for the Joint European Platform for Photonic Integration of Components and Circuits, it is a brokering organisation which helps organizations around the globe to gain access to advanced fabrication facilities for Photonic Integrated Circuits. It aims for low-cost development of application specific InP and TriPleX PICs using generic foundry model, and rapid prototyping via Multi-Project Wafer runs. It collaborates closely with Europe's key players in the field of photonic integration, including manufacturing and packaging partners, photonic CAD software partners, R&D labs and photonic IC design houses.

The JePPIX Roadmap for 2015 has just been published. Visit www.jeppix.eu for your copy.

Photonic integration combining InP and TriPleX™ technologies



At Photonics West last month, a consortium of six companies, including PHASTFlex partner LioniX, demonstrated a new photonic integration design and packaging platform allowing complex optical systems to be embedded into a miniaturised assembly by combining InP and TriPleX PICs. The platform allows for high feature density and high-port-count coupling between the chips, critical advantages in applications like sensing, biophotonics, telecom/datacom and microwave photonics. Success in the PHASTFlex project can enhance this approach significantly.

For more information go to www.lionixbv.nl/lionix-news/press-releases

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